A CMOS REALIZATION OF INVERTING SECOND GENERATION CURRENT CONVEYOR ‘POSITIVE’ (ICCII+)

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ABSTRACT
A CMOS inverting type second generation current conveyor ‘positive’ (ICCII+) is presented which is based on voltage and current mirror circuits. PSPICE simulation results of the proposed structure using 0.5 µm MIETEC CMOS process parameters show that it is suitable for wideband applications and has got a wide output current swing with small current tracking error.

1. INTRODUCTION
Current-mode circuits have received significant attention due to their advantages compared to voltage-mode circuits in terms of inherently wide bandwidth, greater linearity, wide dynamic range, simple circuitry and lower power consumption [1]. Furthermore, current-mode circuits are suitable for integration with CMOS technology and thus become more and more attractive in electronic circuit designs in recent years. At present, a number of current-mode circuit techniques, such as current conveyors (CCs) [2,3], operational transconductance amplifiers (OTAs) [4,5] and four terminal floating nullors (FTFNs) [6,7], have been developed. In these techniques the CCs have proved to be a functionally flexible and versatile current-mode building block. Second generation current conveyors (CCIIs) have found wide use in variety of realizations of active network elements and current-mode circuits. For voltage-mode circuits the electrical variables, for example, the input-output variables are voltage whereas in current-mode circuits these quantities are selected as current. The classical voltage amplifier with its high impedance input and low impedance output is a suitable element for voltage-mode circuits. The current conveyor, however, with its one high impedance (ideally infinite) input, one low impedance (ideally zero) input and one high impedance output is a suitable element for both voltage-mode and current-mode circuits [8,9].

Recently, a new type current conveyor, an inverting type second generation current conveyor (ICCII), has been presented in the literature [10] and its usefulness in the design of active filters and oscillators has been illustrated [11-14]. As explained in [10], various CMOS implementations of ICCII could be considered. For implementing ICCII+, the differential difference current conveyor (DDCC) [15] and the differential voltage current conveyor (DVCC) [16] are employed [11,12].

The purpose of this work is to give a simple and high performance CMOS ICCII+ topology suitable for VLSI technology. The proposed CMOS circuit is based on voltage and current mirror circuits.

2. PROPOSED CIRCUIT
The inverting second generation current conveyor ‘positive’ (ICCII+), whose electrical symbol is shown in Fig. 1(a), has the following port relation between terminal voltages and currents

\[
\begin{bmatrix}
    i_Y \\
    v_X \\
    i_Z \\
\end{bmatrix} = \begin{bmatrix}
    0 & 0 & 0 \\
    -1 & 0 & 0 \\
    0 & 1 & 0 \\
\end{bmatrix} \begin{bmatrix}
    v_Y \\
    i_X \\
    v_Z \\
\end{bmatrix}
\]

(1)

It has negative \(v_X\) and positive \(i_Z\) related to \(v_Y\) and \(i_X\) respectively. It can be represented using a voltage mirror connected to a current mirror as shown in Fig. 1(b) [10].

![Figure 1. ICCII+ (a) symbol representation and (b) mirror representation](image-url)
The CMOS realization of ICCII+ is based on the block diagram shown in Fig. 2(a). The input stage is formed by blocks \( g_{m1} \) and \( g_{m2} \), which are single input single output transconductances. The next stage is a voltage follower stage with a gain of +1 producing X terminal. A negative feedback is used in order to minimize the input impedance at the X terminal. The current mirrors at the output stage convey the current passing through X terminal to Z terminal. The gain between the Y and X terminals depends on the transconductances \( g_{m1} \) and \( g_{m2} \) which must be equal in order to have an inverting property with unity gain between the two transconductances [10].

The proposed CMOS realization of ICCII+ is shown in Fig. 2(b). The circuit is very simple; its input stage is formed by the transistors M1 and M2. For proper performance, the aspect ratios of M1 and M2 must be chosen according to the following relation

\[
\frac{(W/L)_1}{(W/L)_2} = \frac{\mu_p}{\mu_n}
\]

(2)
where $\mu_p$ and $\mu_n$ are the electron and hole mobilities respectively.

Table 1. Transistor dimensions of the proposed ICCII+ circuit

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>W (µm)</th>
<th>L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>43</td>
<td>3.5</td>
</tr>
<tr>
<td>M2</td>
<td>8.1</td>
<td>3.5</td>
</tr>
<tr>
<td>M3</td>
<td>15</td>
<td>1.2</td>
</tr>
<tr>
<td>M4</td>
<td>5</td>
<td>1.2</td>
</tr>
<tr>
<td>M5-M6</td>
<td>15</td>
<td>0.5</td>
</tr>
<tr>
<td>M7-M8</td>
<td>30</td>
<td>0.5</td>
</tr>
<tr>
<td>M9-M12</td>
<td>30</td>
<td>0.5</td>
</tr>
<tr>
<td>M13-M16</td>
<td>15</td>
<td>0.5</td>
</tr>
</tbody>
</table>

The transistors M5- M8 form a translinear loop stage which represents the voltage follower stage of the schematic of Fig. 2(a). The output stage consists of transistors M9-M12 and M13-M16 that they are complementary cascode current mirrors to convey the current passing through the X terminal to Z terminal.

Table 2. 0.5µm MIETEC CMOS process model parameters

```
.MOST NT NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1 VTO=.62 JS=1.8E-6
+XJ=1.5E-6 RS=417 RSH=2.73 LD=0.04E-6 ETA=0
+VMAX=130E3 NSUB=1.71E17 PB=761 PHI=0.905
+THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1
+WD=1.1E-5 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10
+MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10
+CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42
+NFS=1.2E11
.MOST PT PMOS LEVEL=3
+UO=100 TOX=1E-8 TPG=1 VTO=.58 JS=.38E-6
+XJ=0.1E-6 RS=886 RSH=1.81 LD=0.03E-6 ETA=0
+VMAX=113E3 NSUB=2.08E17 PB=911 PHI=0.905
+THETA=0.120 GAMMA=0.76 KAPPA=2 AF=1
+WD=1.1E-6 CJ=85E-5 MJ=0.429 CJSW=4.67E-10
+MJSW=631 CGSO=1.38E-10 CGDO=1.38E-10
+CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81
+NFS=0.52E11
```

3. SIMULATION RESULTS

The proposed CMOS ICCII+ circuit is simulated with the PSPICE program. The MOS transistor aspect ratios are given in Table 1. Table 2 gives device model parameters used for SPICE simulation which are taken from MIETEC 0.5 µm CMOS process. The supply voltages are taken as ±2.5 V. Fig. 3(a) shows the DC relation between Y terminal and X terminal voltages. A linear current following operation over a wide current range can be seen in Fig. 3(b).

Figure 3. DC characteristics of the proposed ICCII+;
(a) $V_X/V_Y$ and (b) $I_Z/I_X$

Figure 4. AC characteristics of the proposed ICCII+;
(a) $V_X/V_Y$ and (b) $I_Z/I_X$
The AC simulation of the circuit shows that the open circuit voltage gain of X terminal has a bandwidth of 814.9 MHz while the short circuit current gain of Z terminal has a bandwidth of 322.6 MHz., as shown in Figs. 4 (a) and (b). The X terminal parasitic input resistance of the proposed circuit is seen to be approximately 60 $\Omega$. The transient analysis of the circuit shows that the total harmonic distortion (THD) is 0.08% at 1 MHz and 0.5 V, peak-to-peak.

4. CONCLUSION

A CMOS realization of ICCII+ has been described. The proposed circuit is based on voltage and current mirror circuits. Simulation results using PSPICE program exhibit that the presented circuit design offers practical alternative solution to use the CMOS ICCII+ in application circuits instead of the CMOS DDCC and DVCC elements. The proposed circuit provides high performance in terms of voltage and current transferring, frequency response and linearity.

5. REFERENCES